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Technology Center 2100

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/852,562
Filing Date: May 10, 2001
Appellant(s): BLAKER ET AL.

David E. Bennett
Registration Number 32194
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is in response to the appeal brief filed 7-3-2006 appealing from the Office action mailed 10-5-2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

NEW GROUND(S) OF REJECTION

The following **new** ground(s) of rejection are applicable to the appealed claims:

Claims 5-10, 14, 34-39, 43, 62-67, and 71 now stand rejected under 35 U.S.C. 103(a) as unpatentable over Hocevar et al., European Patent Application EPO 945 788 A2, and Chi et al., US 5,706,489.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,706,489	Chi et al.	6-1988
6,075,456	Hussain et al.	6-2000
4,763,242	Lee et al.	8-1988

European Patent Application: EP 0 945 788 A2, Hocevar et al., Pub. 9-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

(A) Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(1) Claims 20, 25-29, 49, 54-58, 77, and 82-86 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hocevar.

As for claim 20, Hocevar teaches a method of operating a data processing system (col. 2 lines 5-10) that comprises a host processor (col. 2 lines 5-10: DSP Core processor), a system memory coupled to the host processor (col. 3 lines 47-52: External Memory Interface, col. 4 lines 5-10: the host processor or "DSP Core" is linked to command memory), and an adjunct processor integrated circuit that is coupled to the host processor and the system memory (col. 3 lines 38-40: Co-processor, col. 4 lines 3-9: Reconfigurable hardware co-processor, col. 4 lines 5-10: Co-processor is coupled to host processor or "DSP Core" via a data bus, fig. 1 element 101, the co-processor is linked to command memory as shown in fig. 1 element 141, and is linked to external memory by a data bus as shown in fig. 1 element 101 and as described in col. 5 lines 24-25), the method comprising: providing a command queue in the system memory (col. 5 lines 5-21, col. 5 line 53 through col. 6 line 3: host processor or "DSP Core writes commands to command memory that are stored on a FIFO basis: this comprises a

command queue); loading a command block into the command queue using the host processor (col. 5 line 53 through col. 6 line 3: host processor or "DSP Core writes commands to command memory that are stored on a FIFO basis), the command block comprising an input data field that contains input data (col. 6 lines 19-34: computational commands have an input data field containing memory address for data to be operated on); performing an operation based on the input data using the adjunct processor to generate a result (col. 6 lines 1-34: commands are loaded into command memory by the digital signal processor core and are used to direct the co-processor to carry out operations using the data specified in the input data field); and storing the result in the input data field such that at least a portion of the input data is overwritten (col. 6 lines 49-51: output data may be stored by overwriting the input data at the same address specified by the command data block).

As for claim 25, Hocevar teaches a method of operating a cryptographic data processing system that comprises a host processor (col. 2 lines 5-10: DSP Core processor), a system memory coupled to the host processor (col. 3 lines 47-52: External Memory Interface, col. 4 lines 5-10: the host processor or "DSP Core" is linked to command memory), and a cryptographic processor integrated circuit that comprises a local memory and is coupled to the host processor and the system memory (col. 3 lines 38-40: Co-processor, col. 4 lines 3-9: Reconfigurable hardware co-processor, col. 4 lines 5-10: Co-processor is coupled to host processor or "DSP Core" via a data bus, fig. 1 element 101, the co-processor is linked to command memory as shown in fig. 1

element 141, and is linked to external memory by a data bus as shown in fig. 1 element 101 and as described in col. 5 lines 24-25), the method comprising: providing a command queue in the: system memory (col. 5 lines 5-21, col. 5 line 53 through col. 6 line 3: host processor or "DSP Core writes commands to command memory that are stored on a FIFO basis: this comprises a command queue); providing a read address for the command queue and a write address for the command queue (col. 6 lines 19-55); loading a random number sample into the command queue using the cryptographic processor beginning at the write address; and reading the random number sample using the host processor beginning at the read address (in col. 10 lines 53-58 Hocevar teaches the use of adaptive coefficients as inputs to a processor used in audio and video signal processing. Taught is a method step wherein "there is some feedback path that changes the function over time." Here, Hocevar is referring to a feedback path that is used to determine the coefficients that are used as inputs to functions. In the signal processing associated with audio and video data, this feedback process is used to determine the coefficients needed to be used as inputs to functions implemented by a processor to correct typically random errors introduced into a signal during transmission. The coefficients are themselves randomized by this process. Hocevar teaches this error correction process in col. 11 line 16. The coefficients of Hocevar are taught as being placed into memory along with data in combined memory in col. 4 lines 25-30 and accessible to the crypto co-processor in col. 5 lines 25-30. Therefore, under the adaptive coefficient processing of Hocevar taught in col. 10 lines 53-58, random numbers in the form of adaptive coefficients are loaded into the command queue using

the crypto processor. This is taught inherently by virtue of the fact that input data in the form of the audio or video data is first loaded in block form into data memory before being acted on by the crypto co-processor. Determination of the coefficients to be used by the error correction functions is carried out by the co-processor, and then loaded into shared memory. The adapted coefficients are then directed to be read out and utilized by commands loaded into command memory by the DSP core host processor. The coefficient update process is taught in col. 7 line 51 through col. 18 line 3).

As for claim 26, Hocevar teaches a method as recited in Claim 25, wherein loading the random number sample into the command queue using the cryptographic processor beginning at the write address comprises: determining if the write address plus an amount corresponding to a size of -a single random number sample equals the read address; and loading the random number sample into the command queue using the cryptographic processor beginning at the write address if the write address plus the amount corresponding to the size of the single random number sample does riot equal the read address (col. 5 lines 14-21, col. 6 lines 19-55).

As for claim 27, Hocevar teaches a method as recited in Claim 26, further comprising: incrementing the write address by the amount corresponding to the size of a single random number sample using the cryptographic processor after loading the random number sample into the command queue using the cryptographic processor beginning at the write address if the write address plus the amount corresponding to the

size of the single random number sample does not equal the read address (col. 5 lines 14-21, col. 6 line 19 through col. 7 line 17).

As for claim 28, Hocevar teaches a method as recited in Claim 25, wherein reading the random number sample using the host processor beginning at the read address comprises: determining whether the read address is equal to the write address; and reading the random number sample using the host processor beginning at the read address if the read address is not equal to the write address (col. 5 lines 2-21).

As for claim 29, Hocevar teaches a method as recited in Claim 28, further comprising: incrementing the read address by an amount corresponding to a size of a single random number sample using the host processor after reading the random number sample using the host processor beginning at the read address (col. 5 lines 2-21, col. 6 line 19 through col. 7 line 17).

Claims 49 and 77 recited fundamentally the same limitations as claim 20 and are therefore rejected on the same basis as is that claim

Claims 54 and 82 recited substantially the same limitations as claim 25 and are therefore rejected on the same basis as is that claim.

As for claims 55-58, they recite substantially the same limitations as claims 26-29 respectively, and are therefore rejected on the same grounds as are those claims.

As for claims 83-86, the claims recite substantially the same limitations as claims 26-29 and are therefore rejected on the same basis as those claims.

(2) Claims 15, 44, and 72 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hussain et al., US 6,075,546.

As for claim 15, Hussain teaches A method of operating a cryptographic data processing system that comprises a host processor (col. 3 lines 45-47), a system memory coupled to the host processor (col. 3 lines 53-55), and a cryptographic processor integrated circuit that is coupled to the host processor and the system memory (col. 4 lines 25-33: Rendering Engine and Back-End Graphics processor are taught as components of a "Graphic Processor" This reads on a cryptographic processor by virtue of its ability to undertake graphics processing of the type commonly used in steganography and the watermarking or encoding of graphical data), the method comprising: providing a command queue in the system memory (col. 5 lines 5-10); loading a command block into the command queue using the host processor (col. 5 lines 5-10, 25-45); setting a value of an interrupt field in the command block to request an interrupt when the command block has been executed (col. 5 lines 10-25: Interrupt Variable 208) ; executing the command block using the cryptographic processor (col. 6 lines 17-59) ; and invoking an interrupt using the cryptographic processor after

executing the command block if the interrupt field in the command block is set to the value to request the interrupt (col. 6 line 59 through col. 7 line 6, col. 8 line53-59).

Claims 44 and 72 recite substantially the same limitations as claim 15 and are therefore rejected on the same basis as that claim.

(B) Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(1) Claims 4-10, 12-14, 33-39, 41-43, 61-67, and 69-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hocevar et al., European Patent Application EP0 945 788 A2, and Chi et al., US 5,706,489.

NEW GROUND(S) OF REJECTION:

The rejections of Claims 5-10, 14, 34-39, 43, 62-67, and 71 under 35 U.S.C. 103(a) as unpatentable over Hocevar et al., European Patent Application EPO 945 788 A2, and Chi et al., US 5,706,489, set forth infra, are **new** grounds of rejection.

As for claim 4, Hocevar teaches a method of operating a cryptographic data processing system (col. 2 lines 5-10) that comprises a host processor (col. 2 lines 5-10: DSP Core processor), a system memory coupled to the host processor (col. 3 lines 47-52: External Memory Interface, col. 4 lines 5-10: the host processor or "DSP Core" is linked to command memory), and a cryptographic processor integrated circuit (col. 3 lines 38-40: Co-processor, col. 4 lines 3-9: Reconfigurable hardware co-processor) that comprises a local memory (col. 4 lines 5-10: Co-processor includes command memory, data memory, and coefficient memory) and is coupled to the host processor and the system memory (col. 4 lines 5-10: Co-processor is coupled to host processor or "DSP Core" via a data bus, fig. 1 element 101, the co-processor is linked to command memory as shown in fig. 1 element 141, and is linked to external memory by a data bus as shown in fig. 1 element 101 and as described in col. 5 lines 24-25), the method comprising: providing a command queue in the system memory and loading a command block into the command queue using the host processor (col. 5 lines 5-21, col. 5 line 53 through col. 6 line 3: host processor or "DSP Core writes commands to command memory that are stored on a FIFO basis: this comprises a command queue); executing the command block using the cryptographic processor (col. 4 lines 47-52: host processor or "DSP Core writes commands that direct the co-processor by writing to command memory, col. 5 line 53 through col. 6 line 3), and notifying the host processor that the command block has been executed (col. 13 lines 16-24, an interrupt signal is sent to the host processor or "DSP Core" by the co-processor upon completion of all commands sent to the co-processor). Hocevar does not teach notification of the host

processor of completion of the execution of the command block where the notification comprises updating a completion field in the command block by the co-processor. However, Chi et al. does teach this feature (col. 7 lines 10-17 where a response block field of a command block or "PPB" is used to store a status response sent from a co-processor to a host processor). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Chi et al. into the system of Hocevar. Motive to make this combination is discussed for example, at Hocevar col. 1 lines 35-45 where the advantageous added efficiency of such co-processor signaling is discussed.

As for claim 5, Hocevar teaches a method as recited in Claim 4, further comprising: providing a read address for the command queue and a write address for the command queue (col. 2 lines 20-25col. 4 lines 48-51); wherein loading the command block into the command queue using the host processor comprises loading the command block into the command queue using the host processor beginning at the write address (col. 4 lines 48-51), and wherein executing the command block using the cryptographic processor comprises executing the command block using the cryptographic processor beginning at the read address (col. 5 lines 4-14).

As for claim 6, Hocevar teaches a method as recited in Claim 5, wherein loading the command block into the command queue using the host processor beginning at the write address comprises: determining if the write address plus an amount corresponding

to a size of a single command block equals the read address; and loading the command block into the command queue using the host processor beginning 'at the write address if the write address plus the amount corresponding to the size of the single command block does not equal the read address (col. 5 lines 14-21, col. 6 lines 19-55).

As for claim 7, Hocevar teaches a method as recited in Claim 6, further comprising: incrementing the write address by the amount corresponding to the size of a single command block using the host processor after loading the command block into the command queue using the host processor beginning at the write address if the write address plus the amount corresponding to the size of the single command block does not equal the read address (col. 5 lines 14-21, col. 6 line 19 through col. 7 line 17).

As for claim 8, Hocevar teaches a method as recited in Claim 5, wherein executing the command block using the cryptographic processor beginning at the read address comprises: determining whether the read address is equal to the write address; and executing the command block using the cryptographic processor beginning at the read address if the read address is not equal to the write address (col. 5 lines 2-21).

As for claim 9, Hocevar teaches a method as recited in Claim 8, further comprising: incrementing the read address by an amount corresponding to a size of a single command block using the cryptographic processor after executing the command

block using the cryptographic processor beginning at the read address (col. 5 lines 2-21, col. 6 line 19 through col. 7 line 17).

As for claim 10, Hocevar teaches a method as recited in Claim 4, wherein notifying the host processor that the command block has been executed comprises invoking an interrupt using the cryptographic processor after executing the command block (col. 13 lines 16-33).

As for claim 12, Hocevar and Chi in combination teach the method as recited in claim 4, in addition Chi teaches providing a periodic interrupt, and reading the completion field using the host processor upon invocation of the periodic interrupt (col.4 lines 48-55, col.8 lines 51-60, col.9 lines 55-57). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this feature of Chi into the system of Hocevar. It would be desirable to do so since this would enable the host processor to evaluate the status of command execution by the co-processor.

As for claim 13, Hocevar teaches the method of claim 4, but does not teach setting a timer after loading the command block into the command queue using the host processor, and checking whether the command block has been executed after expiration of the timer. Chi teaches setting a timer after loading the command block into the command queue using the host processor, and checking whether the command block has been executed after expiration of the timer (col.5 line 57 thru col.6 line 3).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Hocevar's data processing system with Chi's method of parallel instruction execution in order to enable database systems to expand accessed records

As for claim 14, Hocevar teaches a method as recited in Claim 4, further comprising: loading at least one operand from the command queue to the local memory; performing at least one operation on the at least one operand to generate a result in the local memory; and storing the result generated in the local memory in the command queue (col. 3 line 38 through col. 4 line 38).

As for claim 33, the claim is directed towards the apparatus that carries out the method of claim 4 and contains substantially the same limitations as that claim. Therefore claim 33 is rejected on the same basis as claim 4.

As for claims 34-39, they recited substantially the same limitations as claims 5-10 respectively, and therefore are rejected on the same basis as claims 5-10.

As for claim 43, the claim recites substantially the same limitation as claim 14 and therefore is rejected on the same grounds as that claim.

As for claim 61, the claim is directed towards a computer program product, embodied in a memory medium, that when read out would cause the system of claim 33

to undertake the method steps of claim 4. Therefore claim 61 is rejected on the same basis as claim 4 and 33.

Claims 62-67 recite substantially the same limitations as claims 4-10 and therefore are rejected on the same basis as those claims.

Claims 41, 42, 69, and 70 recite substantially the same limitations as claims 12 and 13 and therefore are rejected on the same basis as those claims.

As for claim 71, the claim recites substantially the same limitations as claim 14 and therefore is rejected on the same basis as is that claim.

(2) Claims 16,45,73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussain, and further in view of Lee et al (US pat 4,763,242).

As for claim 16, Hussain teaches the method of claim 15, but does not teach storing error information on the command block that is associated with executing the command block using the cryptographic processor. Lee teaches storing error information on the command block that is associated with executing the command block using the cryptographic processor (col.7 lines 1-23). Therefore it would have been obvious to one of ordinary skill in the at the time of the invention to have combined Hussain's packetized command interface with Lee's system providing flexible processor

extension in order to add hardware that extends a computer's processor capability without compromising software compatibility (Lee col.1 lines 9-21, col.2 lines 29-52).

Claims 45 and 73 recite substantially the same limitations as claim 16 and are therefore rejected on the same basis.

(10) Response to Argument

In section A., pages 9 and 10 of his brief, the Appellant asserts that the rejections of independent claims 4, 33, and 61 are improper: arguing that the combination of Hocevar and Chi fail to teach the feature of notification of a host processor that a command block has executed by updating a completion field in the command block using the crypto processor. The Appellant asserts that the cited passages of Chi (col. 7 line 59 through col. 8 line 5; col. 8 lines 42-50, and col. 4 lines 37-47) only teach a halt command for a parallel processor and include no teaching of notification of a host processor that a command block has been executed by updating a completion field. The Appellant asserts that the Header Block **215** of Chi is not used to communicate information from a Parallel Instruction Execution (PIE) facility **120** to a processing unit **110** but "*is instead used to communicate information from the processing unit **110** to the PIE facility **120**.*"

The Examiner counters that a careful reading of Chi reveals that such a feature is indeed taught at the passages cited in the rejection of the claims in the Final Office Action:

In col. 7 lines 10-18, Chi teaches that a crypto co-processor, i.e., the PIE facility, stores a status response for a specific parallel operation. Chi states: "In the preferred embodiment, all zeros in this field indicate that the operation completed normally." This reads very explicitly on the Appellants claim limitation of a crypto co-processor updating a completion field when a command block has been executed.

In col. 4 lines 44-45, Chi teaches that the crypto co-processor (PIE facility) utilizes a PPB response block to communicate a response for an operation just executed, to the host processor, i.e., CPU.

The Appellant appears to have confused the PIE parameter block, which is used to send an instruction from the host processor, i.e., CPU, to the crypto co-processor, i.e. PIE facility (col. 4 lines 39-41), with the message sent back from the PIE facility to the CPU in the form of an updated PPB response block (col. 4 lines 44-47).

In section B, pages 10 and 11 of the brief, the Appellant asserts that the rejections of claims 15, 44, and 72 are improper: arguing that the Hussain reference fails to teach the claimed limitation of a crypto-processor invoking an interrupt after executing a command block if an interrupt field in the command block is set to a value that corresponds to such a request. The Appellant argues that Hussain teaches only a "rendering engine" that only performs address translation as the processor that invokes

the request, and that it is not the graphics processor of Hussain that makes such a request. The Examiner counters by noting that Hussain teaches the "rendering engine" and "back-end graphics processor" as separate components of one "graphics processor' (col. 4 lines 23-35). Therefore this "graphics processor" of Hussain does indeed read on the crypto-processor of the instant application.

In section C, pages 11 and 12 of his brief, the Appellant asserts that the rejections of independent claims 20, 48, and 77 are improper: arguing that Hocevar fails to teach the claimed feature of "performing an operation based on the input data using the adjunct processor to generate a result; and storing the result in an input data field such that at least a portion of the input data is overwritten."

The Examiner counters that a careful reading of Hocevar reveals that such steps are indeed taught (col. 6 lines 1-34: commands are loaded into command memory by the digital signal processor core and are used to direct the co-processor to carry out operations using the data specified in the input data field); and storing the result in the input data field such that at least a portion of the input data is overwritten (col. 6 lines 49-51: output data may be stored by overwriting the input data at the same address specified by the command data block).

In Section D, pages 12 and 13 of his brief, the Appellant asserts that the rejections of independent claims 25, 54, and 82 are improper: arguing that Hocevar fails

to teach the step of loading a random number sample into the command queue and reading the random number sample.

The Examiner counter that a careful reading of Hocevar reveals that such steps are indeed taught, (in col. 10 lines 53-58 Hocevar teaches the use of adaptive coefficients as inputs to a processor used in audio and video signal processing. Taught is a method step wherein "there is some feedback path that changes the function over time." Here, Hocevar is referring to a feedback path that is used to determine the coefficients that are used as inputs to functions loaded as commands into the command queue by the host CPU and utilized by the co-processor to manipulate the input data. In the signal processing associated with audio and video data, this feedback process is used to determine the coefficients needed to be used as inputs to functions implemented by a processor to correct typically random errors introduced into a signal during transmission. The coefficients are themselves randomized by this process. Hocevar teaches this error correction process in col. 11 line 16. The coefficients of Hocevar are taught as being placed into memory along with data in combined memory in col. 4 lines 25-30, and are accessible to the crypto co-processor as taught in col. 5 lines 25-30. Therefore, under the adaptive coefficient processing of Hocevar, taught in col. 10 lines 53-58, random numbers in the form of adaptive coefficients are loaded into the command queue using the crypto processor. This is also taught inherently by virtue of the fact that input data in the form of the audio or video data is first loaded in block form into data memory before being acted on by the crypto co-processor. Determination of the coefficients to be used by the error correction functions loaded into the command

queue is carried out by the co-processor, and then loaded into shared memory. The adapted coefficients are then directed to be read out and utilized by commands loaded into command memory by the DSP core host processor. The coefficient update process is taught in col. 7 line 51 through col. 18 line 3).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

This examiner's answer contains a new ground of rejection set forth in section **(9)** above. Accordingly, appellant must within **TWO MONTHS** from the date of this answer exercise one of the following two options to avoid *sua sponte* **dismissal of the appeal** as to the claims subject to the new ground of rejection:

(1) **Reopen prosecution.** Request that prosecution be reopened before the primary examiner by filing a reply under 37 CFR 1.111 with or without amendment, affidavit or other evidence. Any amendment, affidavit or other evidence must be relevant to the new grounds of rejection. A request that complies with 37 CFR 41.39(b)(1) will be entered and considered. Any request that prosecution be reopened will be treated as a request to withdraw the appeal.

(2) **Maintain appeal.** Request that the appeal be maintained by filing a reply brief as set forth in 37 CFR 41.41. Such a reply brief must address each new ground of

rejection as set forth in 37 CFR 41.37(c)(1)(vii) and should be in compliance with the other requirements of 37 CFR 41.37(c). If a reply brief filed pursuant to 37 CFR 41.39(b)(2) is accompanied by any amendment, affidavit or other evidence, it shall be treated as a request that prosecution be reopened before the primary examiner under 37 CFR 41.39(b)(1).

Extensions of time under 37 CFR 1.136(a) are not applicable to the TWO MONTH time period set forth above. See 37 CFR 1.136(b) for extensions of time to reply for patent applications and 37 CFR 1.550(c) for extensions of time to reply for ex parte reexamination proceedings.

A Technology Center Director or designee must personally approve the new ground(s) of rejection set forth in section (9) above by signing below:

Respectfully submitted,

Conferees:

Kim Vu

SPE

Art Unit 2135

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SUPERVISORY PATENT EXAMIN
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Art Unit 2137